A Scalable MRAM Design Capable of 10Gbits/Chip and Beyond

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In this paper, we present a novel MRAM design that is capable of 50 Gbits/in^2 storage density and beyond with sufficient thermal stability and fabrication tolerance. The design utilizes perpendicular magnetic tunnel junction [1] as the memory element and the word lines and digital lines are arranged as shown in Fig. 1. The design yields $8F^2$ memory cell area assuming the tunnel junction its self is $1F^2$ in area where F denotes the fabrication minimum feature size. Micromagnetic simulations were performed for the element size of 40x40x40 nm^3 to identify the single domain regime where magnetic switching becomes robust with little dependence on possible geometric variation introduced in practical fabrication processes. Noting in the single domain regime, the ratio the perpendicular anisotropy energy constant and saturation magnetization of the storage layer, K/M_S, is the switching field, switching field around 100 Oe can be achieved with sufficient thermal magnetic stability ($\Delta E > 80\ k_BT$) with a material of appropriate perpendicular anisotropy and saturation magnetization as indicated the results in the figure. The design with 40 nm square memory elements will yield close to 50 Gbits/in^2 storage density.

[1]N. Nishimura, et al, J. Appl. Phys., 91, 5246-5249, (2002).